Monday, September 25th

08:20-09:00	**Registration**
09:00-09:30	**Opening**
09:30-10:30	**Keynote Speech: 1** **Plenty of Room at the Bottom? Micropower Deep Learning for IoT end-nodes** **Keynote Speaker: Prof. Luca Benini, Univ.di Bologna,Italy** **Session Chairs: Dr. C.-L. Sotiropoulou, Prof. S. Nikolaidis**
10:30-11:00	**Coffee break**
11:00-12:40	**Session 1** **Non conventional energy efficiency techniques using stochastic and bio-inspired techniques** **Session Chairs: Prof. G. Syrakoulis, Prof. A. Garcia-Ortiz**
25 min	Approximate DIV and SQRT Instructions for the RISC-V ISA: An Efficiency vs. Accuracy Analysis. *Lei Li, Michael Gautschi and Luca Benini* *ETH Zurich, Switzerland*
25 min	FLINT+: A Runtime-Configurable Emulation-Based Stochastic Timing Analysis Framework. *Moritz Weißbrich[1], Guillermo Paya-Vaya[1], Holger Blume[1], Ardalan Najafi[2] and Alberto Garcia-Ortiz[2]* *[1]Institute of Microelectronic Systems, Leibniz Univ. Hannover, Germany [2]ITEM, Univ. of Bremen, Germany.*
25 min	Energy Aware Networks-on-Chip Cortex Inspired Communication. *Erwan Moréac[1], Johann Laurent[1], Pierre Bomel[1], Andre Rossi[2], Emmanuel Boutillon[1] and Maurizio Palesi[3]* *[1]Lab-STICC, Université de Bretagne Sud, France* *[2]LERIA, Université d'Angers, France* *[3]Department of Computer Science and Telecommunications Engineering, Univ. of Catania, Italy.*
25 min	Architecture Exploration of a Fixed Point Computation Unit using Precise Timing Spiking Neurons. *Thomas Mesquida[1], Alexandre Valentian[1], David Bol[2] and Edith Beigne[1]* *[1]Univ. Grenoble Alpes, CEA, LETI, MINATEC Campus, France* *[2]Université catholique de Louvain, Belgium*
12:40-14:00	**Lunch**

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14:00-15:40	**Session: 2** **Three dimensional interconnects: architectures and test** **Session Chairs: Prof. K. Tatas , Prof. K. Siozios**
25 min	Edge Effect Aware Crosstalk Avoidance Technique for 3D Integration. *Lennart Bamberg, Amir Najafi and Alberto García-Ortiz* *ITEM, Univ. of Bremen, Germany*
25 min	3D-IC Signal TSV Assignment for Thermal and Wirelength Optimization. *Yuxin Qian, Cong Hao and Takeshi Yoshimura* *Graduate School of IPS, Waseda Univ. Japan.*
25 min	Embedded Toggle Generator to Control the Switching Activity during Test of Digital 2D-SoCs and 3D-SICs. *Leonidas Katselas[1], Angelos Athanasiadis[1], Alkis Hatzopoulos[1], Hailong Jiao[2], Christos Papameletis[3] and Erik Jan Marinissen[4]* *[1]Aristotle Univ. of Thessaloniki, Greece* *[2]Eindhoven Univ. of Technology, Netherlands* *[3]Cadence Design Systems, USA* *[4]IMEC, Belgium.*
25 min	3DBUFFBLESS: A Novel Buffered-Bufferless Hybrid Router for 3D Networks-on-Chip. *Konstantinos Tatas, Savvas Savva and Costas Kyriacou* *Frederick University, Cyprus*
15:40-16:30	**Poster Session - PhD Forum - Coffee break** **Session Chair: Mr. Ioannis Messaris**
	A Fair Comparison of Adders in Stochastic Regime. *Ardalan Najafi[1], Moritz Weißbrich[2], Guillermo Payá Vayá[2] and Alberto Garcia-Ortiz[1]* *[1]ITEM, Univ. of Bremen, Germany* *[2]Institute of Microelectronic Systems, Leibniz Universität Hannover,Germany*
	Placement-based SER Estimation in the Presence of Multiple Faults in Combinational Logic. *Georgios Ioannis Paliaroutis, Pelopidas Tsoumanis, Georgios Stamoulis and George Dimitriou* *University of Thessaly, Greece*

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	A Topology Optimization Method for Low-Power Logic Circuits with Dual-Threshold Independent-Gate FinFETs. *Haotian Zhu, Jianping Hu, Huishan Yang, Yang Xiong and Tingfeng Yang* *Ningbo University, China*
	Optimal Content-Dependent Dynamic Brightness Scaling for OLED Displays. *Daniele Jahier Pagliari, Enrico Macii and Massimo Poncino* *Politecnico di Torino, Italy*
	Oscillation-based Technique for Post-Bond Parallel Testing and Diagnosis of Multiple TSVs. *Stylianos-Georgios Papadopoulos[1], Vasileios Gerakis[1], Yiorgos Tsiatouhas[2] and Alkis Hatzopoulos[1]* *[1]Aristotle Univ. of Thessaloniki, Greece,* *[2]Univ. of Ioannina, Greece*
	An Analytical Delay Model for ReRAM Memory Cells. *Carola de Benito[1], Rodrigo Picos[1], Mohamad Moner Al Chawa[1], Josep Lluis Rosselló[1], Miquel Roca[1], Spiros Nikolaidis[2] and Ioannis Messaris[2]* *[1]Universitat Illes Balears, Spain* *[2]Aristotle Univ. of Thessaloniki, Greece*
	Power Proportional Adder Design for Internet of Things in a 65 nm Process. *Adrian Wheeldon, Jordan Morris, Danil Sokolov and Alex Yakovlev* *Newcastle University, UK*
	Approximate Adder Segmentation Technique and Significance-Driven Error Correction. *Khaled Al-Maaitah, Ghaith Tarawneh, Ahmed Soltan, Issa Qiqieh and Alex Yakovlev* *Newcastle University, UK*
Phd forum	*Fault-Tolerant Routing Methodology for Networks-on-Chip* *S. Savva, Frederic University, Cyprus*

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16:30-18:00	**Session 3** **Energy efficiency for processing elements: architectures and methodologies** **Session Chairs: Prof. V. Oklobdzija, Prof. N. Konofaos**
22 min	Slow and Steady Wins the Race? A Comparison of Ultra-Low-Power RISC-V Cores for Internet-of-Things Applications. *Pasquale Davide Schiavone[1], Francesco Conti[1,2], Davide Rossi[2], Antonio Pullini[1], Michael Gautschi[1], Eric Flamand[1,3] and Luca Benini[1,2]* [1]*ETH Zurich, Switzerland.* [2]*University of Bologna, Italy.* [3]*GreenWaves Technologies*
22 min	Modeling Energy-Performance Tradeoffs in ARM big.LITTLE Architectures. *Evangelos Vasilakis[1], Ioannis Sourdis[1], Vassilis Papaefstathiou[2], Antonis Psathakis[2] and Manolis G.H. Katevenis[2,3]* [1]*Chalmers University of Technology, Sweden* [2]*FORTH-ICS, Greece* [3]*Univ. of Crete, Greece*
22 min	Empirical CPU Power Modelling and Estimation in the gem5 Simulator. *Karunakar Reddy Basireddy[1], Matthew J. Walker[1], Domenico Balsamo[1], Stephan Diestelhorst[2], Bashir M. Al-Hashimi[1] and Geoff V. Merrett[1]* [1]*University of Southampton, UK* [2]*ARM Ltd., UK*
22 min	uDMA: An Autonomous I/O Subsystem For IoT End-Nodes. *Antonio Pullini[1], Davide Rossi[2], Germain Haugou[1] and Luca Benini[1,2]* [1]*ETH Zurich, Switzerland.* [2]*Univ. of Bologna, Italy.*

Tuesday, September 26th

08:20-09:00	**Registration**
09:00-10:00	**Keynote Speech: 2** **Fast and Accurate CPS Simulation for the masses** **Keynote Speaker: Prof. Ioannis Papaefstathiou,** **Technical Univ. of Crete, Greece.** **Session Chairs: Prof. A. Hatzopoulos, Prof. G. Tsiatouhas**
10:00-10:20	**Coffee break**
10:20-11:35	**VARI Special Session** **Session Chairs: Dr. Nadine Azemard, Prof. D. Soudris**
25 min	Variability and Sensitivity to Process Parameters Variations in InGaAs Dual-Gate Ultra-Thin Body MOSFETs: A Scaling Perspective. *Nicolò Zagni, Francesco Maria Puglisi, Giovanni Verzellesi and Paolo Pavan* *Università di Modena e Reggio Emilia, Italy*
25 min	Effect of Supply Voltage on Random Telegraph Noise of Transistors under Switching Condition. *Mahfuzul Islam[1] and Hidetoshi Onodera[2]* *[1]The University of Tokyo, Japan* *[2]Kyoto University, Japan*
25 min	Optical sensor process variability in a 0.18 µm high voltage CMOS technology. *Frederic Roger, Anderson Singulani and Jong Mun Park* *ams A.G., Austria*
11:35-11:50	**Short break**
11:50-13:05	**Session 4** **Novel technologies for high-performance, low-power and reliability** **Session Chairs: Dr. C.L. Sotiropoulou, Prof. S. Nikolaidis**
25 min	Human α-thrombin detection platform using aptamers on a silicon nanowire FET. *Lotta Römhildt[1], Felix Zörgiebel[1], Bergoi Ibarlucea[1,2], Sebastian Pregl[3], Maryam Vahdatzadeh[1], Walter M. Weber[2,3], Thomas Mikolajick[2,3], Jörg Opitz[4], Larysa Baraban[1,2] and Gianaurelio Cuniberti[1,2]* *[1]Institute for Materials Science, Max Bergmann Center of Biomaterials, Dresden Univ. of Technology.* *[2]Center for Advancing Electronics Dresden, Dresden Univ. of Technology, Germany.* *[3]NaMLab GmbH, Germany.* *[4]Fraunhofer Institute for Ceramic Systems and Technologies, Germany.*

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25 min	Suitability of FinFET introduction into eDRAM cells for operate at sub-threshold level. *Esteve Amat, Antonio Calomarde, Ramon Canal and Antonio Rubio* *Universitat Politecnica de Catalunya, Spain*
25 min	Failure Probability of a FinFET-based SRAM cell utilizing the Most Probable Failure Point. *Michail Noltsis[1], Eleni Maragkoudaki[1], Dimitrios Rodopoulos[2], Francky Catthoor[2] and Dimitrios Soudris[1]* *[1]National Technical University of Athens, Greece* *[2]imec, Belgium*
13:05-14:10	**Light Lunch**
14:30-18:30	**Visit to Royal Tomb of Phillip II**
19:30-	**Conference Dinner**

Wednesday, September 27th

08:20-09:00	**Registration**
09:00-10:00	**Keynote Speech: 3** **Nonlinear Dynamics of Memristor Circuits in Locally Coupled Networks** **Keynote Speaker: Prof. Ronald Tetzlaff, TU Dresden, Germany** **Session chairs: Dr. Alon Ascoli, Prof. Dalibor Biolek**
10:00-10:45	**Poster Session - Coffee break** **Session Chair: Mr. Ioannis Messaris**
	An FPGA-based Thermal Emulation Framework for Multicore Systems. *Md Shahidul Alam[1] and Alberto Garcia-Ortiz[2]* *[1]Univ. of Applied Sciences Bremerhaven, Germany* *[2]ITEM, University of Bremen, Germany*
	Rapid Power-Management Exploration Using Post-Processing of the System-Level Simulation Results. *Dominik Macko* *Slovak Univ. of Technology in Bratislava, Slovakia*
	Timing Modeling at RT-level by Separation of Design - and Stress Related Aging Impacts. *Nils Koppaetzky[1], Malte Metzdorf[1], Reef Eilers[1], Domenik Helms[1] and Wolfgang Nebel[1,2]* *[1]OFFIS Institute for Information Technology Germany* *[2]University of Oldenburg, Germany*
	User dependent Aging Prediction Model for Automotive Controllers with Power Electronics. *Sunil Malipatlolla[1], Ahmet Unutulmaz[2], Domenik Helms[1] and Wolfgang Nebel[1,3]* *[1]OFFIS Institute for Information Technology, Germany* *[2]Previously at OFFIS - Institute for Information Technology* *[3]University of Oldenburg, Germany*
	A Substrate Noise Reduction Methodology Based on Power Domain Separation of GALS Subcomponents. *Milan Babic[1] and Milos Krstic[2]* *[1]BTU Cottbus-Senftenberg, Germany,* *[2]IHP, Germany*

Wednesday, September 27th

	From Edge To Cloud: Design and Implementation of a Healthcare Internet of Things Infrastructure. *Dimosthenis Masouros[1], Ioannis Bakolas[1], Vasileios Tsoutsouras[1], Kostas Siozios[2] and Dimitrios Soudris[1]* *[1]National Technical University of Athens, Greece* *[2]Aristotle University of Thessaloniki, Greece*
	Capacitive Adiabatic Logic based on gap-closing MEMS devices. *Ayrat Galisultanov[1], Yann Perrin[1], Hatem Samaali[2], Louis Hutin[1], Herve Fanet[1], Philippe Basset[2] and Gael Pillonnet[1]* *[1]CEA LETI, France,* *[2]Univ. Paris-Est, ESYCOM, ESIEE Paris, France*
	1-D Memristor-based Cellular Automaton for PseudoRandom Number Generation. *Rafailia-Eleni Karamani[1], Vasileios Ntinas[1], Ioannis Vourkas[2] and Georgios Ch. Sirakoulis[1]* *[1]Department of Electrical and Computer Engineering, Democritus Univ. of Thrace, Greece,* *[2]Pontificia Universidad Catolica de Chile, Chile*
10:45-13:00	**Special Session on Memristors** **Session chairs: Prof. Ronald Tetzlaff, Dr. Alon Ascoli**
22 min	Memristive Two-Ports. *Dalibor Biolek[1], Zdenek Biolek[2] and Viera Biolkova[2]* *[1]UD Brno, Czech Republic* *[2]Brno Univ. of Technology, Czech Republic*
22 min	On the Origin of the Fading Memory Effect in ReRAMs. *Stephan Menzel[1], Anne Siemon[2], Camila La Torre[2], Michael Schulten[2], Rainer Waser[1,2], Alon Ascoli[3] and Ronald Tetzlaff[3]* *[1]Forschungszentrum Juelich, Germany* *[2]RWTH Aachen, Germany* *[3]TU Dresden, Germany*
22 min	Prototyping Memristors in Digital System with an FPGA-Based Testing Environment. *Daniel Wust[1], Mehrdad Biglari[2], Johannes Knödtel[2], Marc Reichenbach[2], Christopher Soell[2] and Dietmar Fey[2]* *[1]Friedrich-Alexander-Universität Erlangen-Nürnberg, Computer Architecture, Germany,* *[2]University Erlangen-Nuremberg, Germany*

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22 min	Memristive Logic: A Framework for Evaluation and Comparison. *John Reuben[1], Rotem Ben Hur[1], Nimrod Wald[1], Nishil Talati[1], Pierre-Emmanuel Gaillardon[2], Shahar Kvatinsky[1] and Ameer Haj Ali[1]* *[1]Technion-Israel Institute of Technology, Israel, [2]Univ. of Utah, USA*
22 min	Parasitic Effects on Memristive Logic Architecture. *Xiaohan Yang, Adedotun Adeyemo, Anu Bala and Abusaleh Jabir* *Department of Computing & Communication Technologies, Oxford Brookes Univ., UK.*
22 min	Pulse Controlled Memristor-based Delay Element. *Thanasin Bunnam[1], Ahmed Soltan[1], Danil Sokolov[1] and Alex Yakovlev[1]* *[1]School of Electrical and Electronic Engineering, Univ. of Newcastle upon Tyne, UK.*
13:00-14:20	**Lunch**
14:20-15:26	**Session 5** **Power and timing modeling for new technologies and logic architectures.** **Session Chairs: Prof. Dietmar Fey, Prof. N. Konofaos**
22 min	Analytical Hold timing fixing for Sub-Threshold Circuit Based on its Lognormal Distribution. *Jingjing Guo, Min Wang, Jizhe Zhu, Xinning Liu and Jun Yang* *Southeast University, China*
22 min	Temperature and Process-Aware Performance Monitoring and Compensation for an ULP Multi-Core Cluster in 28nm UTBB FD-SOI Technology. *Alfio Di Mauro[1], Davide Rossi[2], Antonio Pullini[1], Philippe Flatresse[3] and Luca Benini[1,2]* *[1]ETH Zurich, Switzerland.* *[2]Univ. Of Bologna, Italy.* *[3]ST Microelectronics, France.*
22 min	Evaluation of Single-Phase Clocked Flip Flops at Near-Threshold Voltage Operation. *Yunpeng Cai[1], James Myers[2], Anand Savanth[2], Pranay Prabhat[2], Tom Kazmierski[1] and Alex Weddell[1]* *[1]Univ. of Southampton, UK* *[2]ARM Ltd, UK*

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15:26-15:50	**Coffee break**
15:50-17:20	**Session 6** **Circuits and architectures for power and performance optimization** **Session Chairs: Prof. G. Theodoridis, Prof. M. Dasygenis**
22 min	High-Throughput FPGA Implementation of the CCSDS 122.0-B-1 compression standard. *Nikolaos Kefalas and George Theodoridis* *Univ. of Patras, Greece*
22 min	Parallelization and energy evaluation of interframe compression technique for video images – QSDPCM. *Dimosthenis C. Tsouros, Panagiotis N. Smyrlis and Minas Dasygenis* *Univ. of Western Macedonia, Greece*
22 min	High Voltage Recycling Scheme to Improve Power Consumption of Regulated Charge Pumps. *Steve Ngueya Wandji[1], Jean-Michel Portal[1], Hassen Aziza[1], Julien Mellier[2] and Stephane Ricard[2]* *[1]Aix Marseille Univ, Université de Toulon, CNRS, IM2NP, Marseille, France* *[2]Safran-Starchip, France*
22 min	Investigating the Robustness of Novel Power Analysis Attack Resilient Adiabatic Logic against PVT Variations. *Himadri Singh Raghav, Vivian Bartlett and Izzet Kale* *Univ. of Westminster, UK*
17:20-17:50	**Awards - Closing ceremony**